THE TITLE OF THE INVENTION

Please amend the title of the invention to read as follows.

SEMICONDUCTOR DEVICE HAVING WIRING PATTERNS AND DUMMY PATTERNS COVERED WITH INSULATING LAYER

IN THE SPECIFICATION

Please replace the paragraph beginning at line 2 of page 14 with the following rewritten paragraph:

--The fourth embodiment is described below with reference to Fig. 6. Referring to Fig. 6, a pair of inner and outer dummy patterns 500a, 500b (a third dummy pattern and a first dummy pattern) are formed in the dummy area. Each dummy pattern has a same width (Lw), and formed in the same method with the same size described in the first embodiment. The length (Ls2) between the dummy patterns 500a, 500b is designed for over 0.9 μm. --

Please replace the paragraph beginning at line 15 of page 14 with the

following rewritten paragraph:

-- The fifth embodiment is described below with reference to Figs. 7A and 7B. A bonding pad 601 is formed in a circuit area, and an outer dummy pattern 600b (a first dummy pattern) is formed in a dummy area. The size, location and manufacturing process of the outer dummy pattern is the same as the dummy pattern described in the first embodiment. That is, a width of the outer dummy pattern is designed for 1 μm, and the length (L) is designed for 10 μm. A frame-shaped fourth dummy pattern 600a is formed for surrounding the bonding pad 601 in the circuit area. The distance (Ls3) between the bonding pad 601 and the fourth dummy pattern 600a or the outer dummy pattern 600b is designed for over 0.9 μm. The distance (Ls1) between the metalized wiring pattern 600 and the fourth dummy pattern 600a is designed for over 0.5 μm because of the same reason described in the first embodiment. The metalized wiring pattern 600, the outer dummy pattern 600b and the fourth dummy pattern 600a are formed simultaneously by etching a conductive layer. --